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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,068	07/30/2003	Tae-Seong Jang	SAM-0447	9449

7590 01/26/2005

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EXAMINER	
NGUYEN, VIET Q	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,068	JANG ET AL.	
	Examiner	Art Unit	
	Viet Q Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-8 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 6-8 is/are allowed.

6)☒ Claim(s) 1 and 5 is/are rejected.

7)☒ Claim(s) 2-4 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims **1-8** are present for examination.

Claim Rejections - 35 USC § 103

1. Claims **1 and 5** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Akita et al (6,452,833) and Hoya et al (6,493,251).**

Akita (see Fig.1) clearly shows a semiconductor memory device having a memory cell array (1)), bitline (BL), complementary bit line (bBL), a coupling capacitor (C1, C2) coupling to one end of either bitline or complementary bit line, a bitline sensing amplifier (S/A), a control circuit (see driver 13 or 14) for generating appropriate control signal to the other end of the coupling capacitor (C1 or C2), respectively. However, Fig.8 further shows that the driver circuit (13 or 14) is an inverter receiving an internal power supply from the Vpp/Vcc terminal indirectly. Since the source of transistor (42), as part of the inverter, is receiving a "drop-down" voltage from the Vpp/Vcc through the transistor (41), this received voltage must be "smaller" than the external voltage Vpp/Vcc. Therefore, it would be obvious from the drawing that the internal voltage used by the inverter circuit is a "dropping" from the external voltage Vcc/Vpp as claimed. Further, Vcc/Vpp is also used to power the sensing amplifier as inherently known in this art.

Similarly, **Hoya et al (see Fig. 10)** clearly shows a semiconductor memory device having a memory cell array (MCB1, MCB0), bitline (BL), complementary bit line

(BBL), a coupling capacitor (CA or CB) coupling to one end of either bitline or complementary bit line, a bitline sensing amplifier (S/A 2, see Fig.2), a control circuit (inverters G101 to G104 in combination with driver gates QN21 to QN24)) for generating appropriate control signal to the other end of the coupling capacitor (CA or CB), respectively. However, Fig.10 further shows that the driver/inverter circuits capable of internally switching four different internal power voltages (from V0 to 3V0), generated from the Vpp/Vcc terminal indirectly. Therefore, it would be obvious from the drawing that the internal voltage used by the inverter circuits is a plurality of internal "droppings" from the external voltage Vcc/Vpp, if any existed, as claimed. Further, Vcc/Vpp is also used to power the sensing amplifier as inherently known in this art

2. Other claims are allowable over prior arts of record. Particularly, claim 6 recited the use of "**mode register**" which is lack in the cited prior arts.

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Viet Q Nguyen whose telephone number is (571) 272-1788. The examiner can normally be reached on 7am-6pm (EST).

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Viet Q Nguyen
Primary Examiner
Art Unit 2818

V. Nguyen
1/22/2005